Application No.: 10/616,962 Docket No.: 21806-00113-US1

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method of forming a crystalline polysilicon gate electrode structure on a gate dielectric, the method comprising:

depositing, on the gate dielectric, polysilicon crystals of substantially a first size; ~~and~~

cooperatively selecting a second grain size in conjunction with the first size so as to maximize a dopant activation in a region near the gate dielectric; and

contiguously with the crystals of the first size, depositing directly thereon additional polysilicon crystals of substantially ~~a~~ the second size.

2. (Original) The method according to claim 1, wherein:

the first crystal size is larger than the second crystal size.

3. (Original) The method according to claim 1, wherein:

the first crystal size is smaller than the second crystal size.

4. (Currently amended) A method of forming a crystalline polysilicon gate electrode structure on a gate dielectric, the method comprising:

controlling a variation of at least one of temperature, pressure, and flow rate of a

continuous flow of silane or related silicon precursor species while depositing polysilicon therefrom as crystals of correspondingly controlled grain size; and

forming a multi-region polycrystalline silicon deposition having regions with crystals of respectively different grain sizes by controlling said variation.

5. (Currently amended) The method according to claim 4, wherein:

the variation is controlled in a step-wise manner, ~~to thereby form~~ and a multi-region polycrystalline silicon deposit is formed comprising regions having crystals of respective grain sizes.

6. (Original) The method according to claim 5, ~~wherein:~~ wherein, during said depositing polysilicon,

crystals deposited in a first region adjacent to the gate dielectric have a first grain size selected to maximize dopant activation near the gate dielectric and a second region ~~that~~ has crystals of a second grain size deposited more distantly from the gate dielectric.

7. (Currently amended) A method of forming a polycrystalline silicon structure in which crystal grain size varies as a function of depth, the method comprising:

controlling a variation of at least one of temperature, pressure, and flow rate of a silane gas while depositing silicon therefrom, ~~to thereby control~~ on a substrate; and

controlling the crystal grain size as a function of depth in the ~~deposited~~ polysilicon structure; and

forming a plurality of regions having respective different grain sizes.

8. (Canceled).

9. (Currently amended) The method according to claim ~~8~~7, wherein:

the polycrystalline silicon structure is a gate electrode formed on a gate dielectric, and comprises a first region having a first crystal grain size and a second region formed thereon and having a second grain size,

wherein the first and second grain sizes are selected to maximize dopant activation in the first region and to achieve a specific resistance in the second region.

10. (Currently amended) The method according to claim 9, further comprising:

depositing a third region ~~formed~~ on the second region ~~and~~ having crystals of a third grain ~~size, to~~size so as to further tailor the specific resistance of the gate ~~conductor structure~~electrode.

11. (Currently amended) The method according to claim ~~8, wherein: the~~7, further comprising controlling a pressure of the silane gas so as to vary an electrical resistance of the deposited silicon ~~varies~~ inversely with the controlled pressure.

12. (Previously presented) The method according to claim 7, further comprising:

providing a controlled flow of a dopant gas during a selected portion of the step of depositing polysilicon, to thereby enable selected doping or counter-doping of a portion of the deposited polysilicon.

13. (Original) The method according to claim 12, wherein:

the dopant gas is selected to provide one of a p-type or an n-type doping during a final portion of the step of depositing polysilicon.

14. (Previously presented) The method according to claim 7, further comprising:

forming a layer rich in carbon atoms at a selected stage of the silicon deposition.

15. (Previously presented) The method according to claim 7, further comprising:

forming a layer of silicon-germanium at a selected stage of the silicon deposition.

16. (Original) The method according to claim 7, wherein:

the variation is controlled to deposit the polysilicon so that the crystal grain size varies monotonically during the deposition of the polysilicon.

Claims 17-22 (Cancelled)

23. (Previously presented) A CMOS transistor, comprising:

a dielectric film;

a gate conductor on the dielectric film,

wherein the gate conductor includes a region of polycrystalline silicon,

said region of polycrystalline silicon having a continuously varying grain size as a function of a distance measured from a surface of the dielectric film.

24. (Previously presented) The CMOS transistor of claim 23, wherein said continuously varying grain size decreases continuously as a function of the distance measured from a surface of the dielectric film.

25. (Previously presented) The CMOS transistor of claim 23, wherein said continuously varying grain size increases continuously as a function of the distance measured from a surface of the dielectric film.

26. (New) The method of claim 4, wherein said forming a multi-region polycrystalline silicon deposition comprises forming at least first, second, and third regions having respective crystal grain sizes.

27. (New) The method of claim 26, wherein the first and second regions are separated by the second region, and wherein the first and third regions have respective grain sizes which are essentially equal.